AMENDMENTS TO THE SPECIFICATION

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED REVISION TO 37 CFR 1.121)

Please replace the paragraph beginning at page 5, line 9 with the following paragraph:

A1

Referring to FIG. 4, a detailed block diagram of the delay circuit 101 is shown. The delay circuit 101 may be implemented, in one example, within ~~an~~ a JTAG port. The delay circuit ~~100~~ 101 may comprise a high speed transceiver logic ~~(HTSL)~~ (HSTL) block (or circuit) 108, a plurality of delay blocks (or circuits) 109a-109n, and a switch 111. The ~~HTSL~~ HSTL circuit 108 may be compliant with the JEDEC specification for input/output interfaces, which is hereby incorporated by reference in its entirety~~)~~. The ~~HTSL~~ HSTL circuit 108 may be programmed to implement a variety of common applications. For example, the ~~HTSL~~ HSTL circuit 108 may be programmed to control data input to the delay blocks 109a-109n. HSTL is the JEDEC standard for input/output interfaces in low voltage designs (e.g., 2.5V and under). Since the voltage swings on HSTL inputs and outputs are much smaller (e.g., 0-1.5V range with rise and fall times of 0.5ns (edge rates of 2v/ns)), appropriate setup/hold timing is important.

A1 end

However, the present invention is applicable to other technologies, such as TTL, CMOS, etc.

Please replace the paragraph beginning at page 7, line 20 with the following paragraph:

A2

~~The~~ Referring to FIG. 3 in conjunction with FIG. 4, the circuit 100 generally starts operation when the signal is presented to the delay block 101. The delay block 101 may provide a data delay (e.g., the signal DIN_DLY) of the input data DIN. The register 102 may receive the delayed data signal DIN_DLY. Additionally, the register 102 may present the signal DOUT in response to the clock CLK. A particular delay length of the signal DIN may be determined in response to the signal S_H. The switch 111 may determine which delay circuit 109a-109n to select in response to the signal S_H. The signal S_H may be implemented, in one example, as a user configuration setup and hold timing signal. In another example, the signal S_H may be implemented as a multi-bit signal. The delay circuits 109a-109n may each be implemented with a different delay length. The data input DIN may be delayed according to a selection of an appropriate delay (e.g., the delay circuits 109a-109n).